REMARKS

Claims 1-7, 16 and 17 stand rejected. Claims 8-13 and 18-21 have been allowed. More particularly, claims 1-7 and 16-17 stand rejected under 35 U.S.C. 103(a). Appreciation is again expressed at this time for the allowance of claims 8-13 and 18-21. Claim 1 has been amended. The Examiner's rejection of claims 1-7 and 16-17 are addressed below. Reconsideration of the application is respectfully requested.

Rejections Under 35 U.S.C. 103(a)

The Examiner rejected claims 1, 3-7, 16 and 17 under 35 U.S.C. 103 as being unpatentable over U.S. Patent No. 6,747,325 to Shih in view of U.S. Patent No. 6,566,204 to Wang et al. The Examiner concedes that Shih does not disclose the halo implantation of multiple devices. To supply the missing subject matter, the Examiner has cited to Wang et al.

The combination of the Shih and Wang references is problematic for several reasons. To begin with, the skilled artisan considering the combined teachings of the Shih and Wang et al. references would face a considerable conundrum. On the one hand, the Shih reference discloses a fabrication process involving a single transistor.[1] On the other hand, the Wang et al. reference discloses usage of a mask to perform multiple halo implants.[2] However, Wang et al. discloses the multiple halo implants using a mask wherein the multiple implants are substantially perpendicular to the first two performed implants. In other words, and taking FIG. 14 as an example, two implants are performed with an azimuthal angle β_1 and β_2 and then subsequent implants are performed at azimuthal angles β_3 and β_4. But note that the implant 216′ performed at angle β_3 is substantially perpendicular to the implant 218 performed at angle β_2. This, of course, directly contrasts with the language of claim 1 that provides that the halo regions are formed without implanting in a direction

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[1]Shih, col. 6, ll. 2-17.

[2]Wang et al., col. 22, ll. 31-40 and FIG. 14. Wang et al. does contemplate a halo process for a single transistor. *See* Wang et al., col. 28, ll. 30-38. However, Wang et al. does not disclose halo processing of a single transistor wherein the implanted transistor is substantially aligned with a first axis that is substantially perpendicular to an axis of another device as set forth in claim 1 as amended.

substantially perpendicular to the first and second directions. Thus, the skilled artisan would be strenuously led away from the claimed invention by virtue of the fact that Wang et al. discloses multiple halo implants where the halo regions are formed by implants that are perpendicular as shown in FIG. 14. Accordingly, the combination of Shih and Wang et al. must fail.

Claim 2

Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Shih in view of U.S. Patent No. 6,784,062 to Cho et al. Shih discloses a fabrication process for a thin film transistor (TFT) for controlling pixels of a TFT liquid crystal display.[3] Two embodiments are disclosed that use halo regions.[4] Interestingly, the two embodiments are described solely in the context of an N-type lightly doped drain (LDD) and a P-type halo region. There is no hint or suggestion of using anything other than an N-type LDD and a P-type halo.

Cho et al. discloses a fabrication process to build side-by-side N-channel and P-channel transistors with halo regions using a quad implant process.[5] The stated application for the transistors in Cho et al. is random access memory.[6]

Applicants submit that there is no motivation to combine the teachings of Shih and Cho et al. as required by 35 U.S.C. 103(a). As just noted, Cho et al. discloses subject matter related to quad halo implantation in the random access memory context. Shih discloses a TFT process solely in the context of an N-type LDD and a P-type halo and for a very particularized application, namely, a pixel control for a TFT liquid crystal display. The skilled artisan would simply not be motivated to take the rather specific teachings of Shih and then turn to the otherwise disparate teachings of the Cho et al. reference and plug the same into Shih.[7]

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[3]Shih, col. 1, ll. 14-18.

[4]Shih, col. 6, ll. 2-17, FIGS. 4a-4h, col. 7, ll 56-60 and FIGS. 5a-5h.

[5]Cho et al., col. 3, ll. 44-50.

[6]Cho et al., col. 2, ll. 46-59.

[7]The Examiner has again asserted that Shih and Cho et al. are from the same field of endeavor. August 11, 2006 Office Action ¶4. Applicants submit that this issue is not altogether

Claims 3-7, 16 and 17

The Examiner rejected claims 3-7, 16 and 17 under 35 U.S.C. 103(a) as being unpatentable over Shih in view of Wang et al. For the reasons advanced above with regard to the patentability of claim 1, Applicants submit that claims 3-7, 16 and 17 are similarly patentable.

Conclusion

For the extensive reasons advanced above, Applicants submit that claims 1-13 and 16-21 are patentable and respectfully request that a Notice of Allowability issue in due course.

Miscellaneous

The Commissioner for Patents is authorized to charge any required fees or credit any overpayment to Deposit Account No. 01-0365, Order No. AMDI:133\HON.

Respectfully submitted,

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clear. As noted elsewhere herein, Shih discloses a specific transistor design for use in TFT liquid crystal displays while Cho et al. discloses transistor concepts for use in random access memory devices. Furthermore, Applicants submit that Cho et al. does not disclose processing of a circuit wherein the implanted circuit device is substantially aligned with a first axis that is substantially perpendicular to an axis of another device as set forth in claim 1 as amended.